PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Budge, William et al.

Serial No. : Unknown

Filing Date : Herewith

For : Use of Selective Ozone TEOS Oxide to Create Variable Thickness Layers and Spacers

Attorney Docket No. : MTI-31079-C

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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37 CFR 1.8(a)

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Date: January 31, 2002

Assistant Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

PRELIMINARY AMENDMENT

This application is a divisional of U.S. Serial No. 09/652,188. Prior to calculating the filing fee, please cancel Claims 1-23 and 32-35.

Prior to substantive examination, Applicant requests the following amendments be made in this application.

IN THE SPECIFICATION

Please amend the specification at page 1, by inserting after the title:

--CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. Pat. Application Serial No. 09/652,188, filed August 31, 2000.--

IN THE CLAIMS

Please cancel Claims 1-23 and 32-35. Claim 25 is amended as shown in the attached replacement claims submitted under 37 C.F.R. § 1.121(c). The amendments to Claims 25-29 merely corrects the claim dependencies.

IN THE DRAWINGS

Please replace FIGS. 1-5 with new FIGS. 1-5.

REMARKS

It is respectfully submitted that the claims are in condition for allowance and notification to that effect is earnestly solicited. The Examiner is urged to telephone the undersigned attorney if any questions should arise.

Respectfully submitted,

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Dated: January 31, 2002

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THE INVENTION CLAIMED IS:

24. A semiconductor memory device comprising:

at least one first wordline comprising P-type silicon or polysilicon and a first nonconductive silicon oxide layer;

at least one second wordline comprising N-type silicon or polysilicon and a second nonconductive silicon layer; and

wherein the first layer is thicker than the second layer.

25. The semiconductor memory device of Claim 24, wherein the first and second spacers are formed using tetraethylorthosilicate/ ozone deposition in a one step process.

26. The semiconductor memory device of Claim 24, wherein at least one of the first wordline or the second wordline form part of a DRAM array.

27. The semiconductor memory device of Claim 24 wherein the DRAM array is part of a system-on-chip.

28. The semiconductor memory device of Claim 24, wherein at least one of the first wordline or the second wordline form part of an SRAM array.

29. The semiconductor memory device of Claim 24 wherein the SRAM array is part of a system-on-chip.

30. A multi-gate semiconductor device comprising:

at least one first P-type gate surrounded by a first nonconductive silicon oxide layer; and

at least one second N-type silicon gate surrounded by a second nonconductive silicon oxide layer;

wherein the first nonconductive spacer is thicker than the second nonconductive layer.

31. The multi-gate semiconductor device of Claim 30, wherein the device is part of a logic circuit.

Redlined Claims

THE INVENTION CLAIMED IS:

24. A semiconductor memory device comprising:

at least one first wordline comprising P-type silicon or polysilicon and a first nonconductive silicon oxide layer;

at least one second wordline comprising N-type silicon or polysilicon and a second nonconductive silicon layer; and

wherein the first layer is thicker than the second layer.

25. The semiconductor memory device of Claim ~~25~~ 24, wherein the first and second spacers are formed using tetraethylorthosilicate/ ozone deposition in a one step process.

26. The semiconductor memory device of Claim ~~25~~ 24, wherein at least one of the first wordline or the second wordline form part of a DRAM array.

27. The semiconductor memory device of Claim ~~25~~ 24 wherein the DRAM array is part of a system-on-chip.

28. The semiconductor memory device of Claim ~~25~~ 24, wherein at least one of the first wordline or the second wordline form part of an SRAM array.

29. The semiconductor memory device of Claim ~~25~~ 24 wherein the SRAM array is part of a system-on-chip.

30. A multi-gate semiconductor device comprising:

at least one first P-type gate surrounded by a first nonconductive silicon oxide layer; and

at least one second N-type silicon gate surrounded by a second nonconductive silicon oxide layer;

wherein the first nonconductive spacer is thicker than the second nonconductive layer.

31. The multi-gate semiconductor device of Claim 30, wherein the device is part of a logic circuit.